IN THE CLAIMS:

Claims 1-36 (Cancelled).

37. (Original) A method of preventing a circuit having a test mode entry function from entering a subsequent test mode after said circuit enters a first test mode, comprising:

initiating a test mode blocking signal after said circuit completes said first test mode; and

exclusively controlling said test mode entry function of said circuit with said test mode blocking signal.

38. (Original) The method in claim 37, further comprising generating said test mode blocking signal responsive to a final test latch of said circuit during said first test mode.

39. (Original) The method in claim 38, further comprising originating said test mode blocking signal from said circuit.

Claims 40-51 (Cancelled).

52. (Original) A method of protecting a test circuit from receiving a subsequent latching signal after receiving at least one prior latching signal, comprising:

allowing at least one prior latching signal to reach said test circuit;

performing a test circuit operation for each prior latching signal;

providing a lockout signal; and

stopping any subsequent latching signal with said lockout signal.

53. (Original) The method in claim 52, wherein providing said lockout signal further comprises generating said lockout signal responsive to a last prior latching signal.

54. (Original) A method of preventing a test vector decode circuit from reentering a test mode, comprising:

making a reentry into said test mode dependent upon a change of an output vector of said test vector decode circuit; and

making said change of said output vector dependent upon said reentry into said test mode.